Roll No. | | | | | | | | | | | | | **Total No. of Pages : 01**

Total No. of Questions : 08

M.Tech (CSE) (2018 Batch) (Sem.–3)

COMPILER FOR HPC

Subject Code : MTCS303-18

M.Code : 76510

Date of Examination : 21-12-22

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1.Attempt any FIVE questions out of EIGHT questions.

2.Each question carries TWELVE marks.

1. Discuss the structure of a compiler required for high performance computing. List the features programming languages for high performance computing.

2. Explain various types of data dependence. What is a program dependence graph? How is it used to evaluate data dependence?

3. Write in detail about the transformations used for loop restructuring: Give appropriate examples for each transformation. Discuss the need of loop restructuring.

4. What is vector analysis? Explain the basic criteria of vectorizable loops. Explain the process of generating vectorized code from sequential loops and from For All loops with the help of examples.

5. Differentiate between SIMD and MIMD machines. Discuss parallel code for array assignment.

6. Write detailed notes on : (a) Local cache coherence, and (b) Concurrency from parallel loops.

7. Discuss the recent trends in compiler design with respect to high performance computing machines and message passing machines.

8. List the applications and challenges in pointer analysis. Explain the process of points- to analysis with the help of examples.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.