Roll No. | | | | | | | | | | | | | **Total No. of Pages : 01**

Total No. of Questions : 08

M.Tech. (VLSI Design) (Sem.–1)

VLSI TECHNOLOGY

Subject Code : MTVL-PE2A-18

M.Code : 75210

Date of Examination : 25-01-23

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1.Attempt any FIVE questions out of EIGHT questions.

2.Each question carries TWELVE marks.

1. a) Describe epitaxial model to grow silicon on silicon wafer.

   b) Describe the wet chemical etching process for silicon dioxide, silicon nitride and polysilicon.

2. a) Describe the coupling between various types of simulation. Discuss Boltzmann transport equation method used to simulate Ion implantation phenomena in solids.

   b) Compare RTP and conventional furnace used for the thermal processing of the films.

3. Discuss the masking sequence and process integration of NMOS using appropriate schematic diagrams.

4. a) What is the failure rate in metal interconnects? How can it be reduced?

   b) Differentiate between evaporation and sputtering.

5. Describe the methods in detail for making a photo mask. What are the defects which may arise during the mask generation?

6. **Write a short note on :**

   a) Clean rooms

   b) High K and low k dielectrics in ULSI

7. Describe One dimensional Fick's Diffusion model in detail.

8. Describe in detail the Deal and Grove's Model for the silicon oxidation.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.