Roll No. | | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 08

M.Tech (VLSI Design) (Sem.–1)

RTL SIMULATION & SYNTHESIS WITH PLD

Subject Code : MTVL-102-18

M.Code : 75206

Date of Examination : 27-01-23

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **Attempt any FIVE questions out of EIGHT questions.**
2. **Each question carries TWELVE marks.**

1. a) Discuss the static timing analysis of a synchronous design.

   b) Explain the design strategies for multi-clock domain designs.

2. a) Explain pre-defined and user-defined attributes of VHDL with the help of suitable examples.

   b) Differentiate between:

   (i) Signals and Variables

   (ii) 'WHEN' and 'CASE' statements

   with suitable examples.

3. Draw the state diagram for a Moore type sequence detector to detect the sequence "11001". Overlapping sequences are accepted. Also write the VHDL code for the obtained state diagram.

4. a) Explain the components of a Verilog Module with block diagram.

   b) Explain in detail about PLA and PAL devices.

5. a) Explain the ASIC design flow with a neat diagram and write the difference between custom IC and standard IC.

   b) What is redundant logic and how it can be tested in a circuit?

6. a) Explain partial and full scan techniques which are used to test physical defects or functional problems.

   b) Explain the use of external hard IP during prototyping.

7. Discuss case studies and speed issues with the help of suitable example.

8. Write short notes on the following (any two) :

   a) Programmable interconnects

   b) BIST

   c) Meta-stability.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.