Roll No. | | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 08

M.Tech (VLSI Design) (Sem.–1)

CMOS VLSI DESIGN CONCEPTS

Subject Code : MTVL-101-18

M.Code : 75205

Date of Examination : 19-01-23

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **Attempt any FIVE questions out of EIGHT questions.**
2. **Each question carries TWELVE marks.**

1. a) Why pMOS and nMOS are sized equally in a transmission gate. Discuss the

   b) What is latch up condition in CMOS circuits? How it can be eliminated?

2. With the help of neat diagrams, discuss the working principle of MOS transistor scaling. What is influence of scaling on interconnect media.

3. a) Differentiate between clock skew and signal skew with suitable examples.

   b) Explain about 2 phase pseudo memory structure.

4. Write the short note on system design of:

   a) Manchester Carry adder

   b) Serial/Parallel multiplier

5. a) Discuss the working of Variable Threshold CMOS circuits. Enlist the uses of VTCMOS technique.

   b) Differentiate between pipelining and parallel processing with suitable examples.

6. a) Briefly outline the needs of low power chip design

   b) What do you understand by charge sharing ? What is the solution to eliminate it

7. Explain the following:

   a) Tristate inverter

b) Delay estimation

c) Components of power dissipation in CMOS

8. The following parameters are given for an nMOS process.

- t_{ex} = 500A
- substrate doping $N_A = 1.10^{16}$ cm^{-3}:
- polysilicon gate deling $N_D = 1.10^{20}$ cm
- oxide-interface fixed-chaise density $N_{ex} = 2.10^{l0}$ cm^{-3}

a) Calculate V_r for an unimplanted transistor.

b) What type and what concentration of impurities must be implanted to achieve V_r = +2Vand V_r = –2V?

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.