Roll No. | | | | | | | | | | | | **Total No. of Pages : 01**

Total No. of Questions : 08

M.Tech (VLSI Design) (Sem.–1)

CAD OF DIGITAL SYSTEM (Elective – I)

Subject Code : MTVL-PE1A-18

M.Code : 75207

Date of Examination : 23-01-23

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **Attempt any FIVE questions out of EIGHT questions.**
2. **Each question carries TWELVE marks.**

1. a) Explain the design methods and technologies for VLSI circuits.

   b) Explain the fabrication process of VLSI devices.

2. a) Explain the different ways of checking the correctness of an integrated circuit without actually fabricating it.

   b) Explain Prim's algorithm for minimum spanning trees with a suitable example.

3. What is Integer Linear Programming (ILP)? Why ILP is useful in CAD for VLSI? Explain ILP with a suitable example.

4. a) Explain partitioning based placement algorithms.

   b) Explain floor planning algorithms for mixed block and cell design.

5. a) Classify global routing algorithms and explain Maze routing algorithm.

   b) Compare Non-rectilinear Steiner tree based algorithm and weighted Steiner tree based algorithm.

6. a) Explain algorithm for street congestion minimization of single row routing problem.

   b) Explain LEA based algorithms of two-layer channel routing algorithms.

7. Classify three layer channel layer algorithms. Compare extended net merge channel router and hybrid HVH-VHV router. Also, explain HVH routing from HV-solution.

8. **Write short notes on the following (any two) :**

   a) Gate array

   b) Group migration algorithms

   c) Steiner tree based algorithms.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.