Roll No. | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

MCA (2015 & Onward) (Sem.–6)

ADVANCED COMPUTER ARCHITECTURE

Subject Code : MCA-603

M.Code : 74757

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. SECTIONS-A, B, C & D contains TWO questions each carrying TEN marks each and students has to attempt any ONE question from each SECTION.
2. SECTION-E is COMPULSORY consisting of TEN questions carrying TWENTY marks in all.

SECTION-A

1. What are the various measures available to evaluate the performance of processors? How do each of these relate to the ultimate measure of performance? Explain.
2. Discuss the various hardware techniques used for handling control and name hazards.

SECTION-B

3. Discuss memory hierarchy in detail.
4. What do you mean by Cache memory? What are the types of cache? Discuss and differentiate between Write-through and Write-back caches.

SECTION-C

5. What is memory disambiguation? Discuss the various memory disambiguation mechanisms.
6. Explain the architecture and working of VLIW processor with the help of a block diagram.

SECTION-D

7. Discuss non-blocking cache memories.
8. What is multiprocessor cache coherence? Illustrate the problem and show how different processors have different value for the same location.

SECTION-E

9. Answer the following in brief :

A. What are single cycle processors?

B. Differentiate between hardwired and micro-coded FSM processors.

C. What is branch hazard?

D. Define RAW, WAW, WAR and RAR hazards.

E. What is dynamic instruction scheduling?

F. Compare cold and warm caches.

G. How is pipelining to cache implemented?

H. What is register renaming?

I. Define Virtualization.

J. What are the problems of multithreading?

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.