Roll No. | | | | | | | | | | | | Total No. of Pages : 2

Total No. of Questions : 09

MCA (2015 & Onward) (Sem.–6)

ADVANCED COMPUTER ARCHITECTURE

Subject Code : MCA-603

Paper ID : [74757]

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. SECTIONS-A, B, C & D contains TWO questions each carrying TEN marks each and students has to attempt any ONE question from each SECTION.
2. SECTION-E is COMPULSORY consisting of TEN questions carrying TWENTY marks in all.
3. Use of non-programmable scientific calculator is allowed.

SECTION-A

1. Explain principles of designing pipelined processors. Calculate efficiency and throughput of pipelined processors.

2. Differentiate between hardwired and micro-coded FSM processors.

SECTION-B

3. What do you mean by Cache? Explain Write-through and Write-back caches.

4. Explain direct mapping and associative mapping techniques.

SECTION-C

5. What is VLIW? Explain its architecture with the help of a block diagram. Also describe the problems associated with VLIW approach.

6. Explain superscalar processors in detail.

SECTION-D

7. Discuss non-blocking cache memories.

8. What is meant by cache coherence problem? Describe various protocols to handle cache coherence.

SECTION-E

9. Answer the following in brief :

a) What are single cycle processors?

b) What are structural hazards?

c) Define RAW, WAW, WAR and RAR hazards.

d) What are the measures of analyzing processor performance?

e) Compare cold and warm caches.

f) How is pipelining to cache implemented?

g) What is register renaming?

h) What does branch prediction mean?

i) Define Virtualization.

j) What are the problems of multithreading?