Roll No. | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 09

B.Voc. (Hardware and Networking) (Sem.–4)

COMPUTER SYSTEM ARCHITECTURE

Subject Code : BVHN-404-18

M.Code : 77483

Date of Examination : 22-12-22

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION–A

1. Answer briefly :

a. Differentiate between SOP and POS.

b. List out the advantages and disadvantages of K-map method.

c. What are called don't care conditions?

d. Differentiate between edge triggering and level triggering.

e. Define combinational logic.

f. Differentiate between a Multiplexer and a Demultiplexer.

g. What is Half adder?

h. Distinguish between latch and flip-flop.

i. What is an Address Bus?

j. Explain Memory Reference Instructions.

SECTION-B

2. Explain about Boolean postulates and laws.

3. What is a multiplexer? Explain with a truth table and logic circuit the design of an 8 to 1-line multiplexer.

4. Write difference between Combinational & Sequential circuits.

5. Explain the working of a JK flip-flop with a truth table and logic circuit.

6. Explain different types of computer registers with common bus system with a neat sketch.

SECTION-C

7. Simplify the following function in SOP and POS using K-Map

   $F(A, B, C, D, E) = \sum m(0, 1, 3, 4, 5, 9, 11, 12, 13, 15)$

8. Design 4-bit binary adder/subtractor.

9. Explain D-Flip flop and T-Flip flop in detail.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.