

Roll No.

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Total No. of Pages : 02

Total No. of Questions : 18

B.Tech. (IT) (2018 Batch) (Sem.-3)

COMPUTER ARCHITECTURE

Subject Code : BTES-302-18

M.Code : 76394

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION-A

Answer briefly :

1. What are addressing mode used for?
2. How a number is represented using floating point representations?
3. Explain pros and cons of RISC architecture.
4. What are different layers of memory organization?
5. What is role of interrupts?
6. What is DMA controller?
7. What is the difference between hardware and software interrupts?
8. What are the disadvantages of multi-level cache memory?
9. Differentiate between write back and write through policies.
10. Why Optimal Page Replacement Algorithm is practically impossible to implement?

SECTION-B

11. Explain in detail differences between hardwired and micro-programmed control unit design.
12. Create the circuit diagram of full adder using two half adders.
13. Explain parallel processing. What are the challenges in achieving parallel processing?
14. Differentiate between primary and secondary memory with examples.
15. Write short note on I/O interfaces.

SECTION-C

16. Explain various stages in instruction pipelining. Discuss in detail methods to handle control hazards.
17. Explain cache mapping techniques viz, Direct, associative and Set-Associative mapping.
18. Explain addressing modes in 8085 microprocessor with examples:
 - a. Immediate addressing mode
 - b. Register addressing mode
 - c. Direct addressing mode
 - d. Register indirect addressing mode
 - e. Implied addressing mode

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.