Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 18

B.Tech (CSE/IT) (Sem.–3)

DIGITAL CIRCUITS & LOGIC DESIGN

Subject Code : BTCS-303

Paper ID : [A1125]

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

Answer briefly :

Q1. Compare combinational with sequential circuits?

Q2. What is the use of parity checker?

Q3. What are Karnaugh Maps?

Q4. Draw a 4*1 multiplexer?

Q5. Write the truth table of JK Flip Flop?

Q6. Draw *T* type of Flip Flop?

Q7. Define edge triggering?

Q8. Discuss read operation in memory?

Q9. What is static RAM cell?

Q10. What is Moore circuit?

SECTION-B

Q11. What are weighted and non weighted codes?

Q12. Design a combination circuits for a full adder and explain it in detail?

Q13. What are shift registers? Explain the shift right operation?

Q14. What is Field Programmable Gate Arrays (FPGAs) and how it is used?

Q15. Explain the principle operation of RTL & DTL?

SECTION-C

Q16. Discuss principle of duality in De-Morgan Theorem. Explain minimization of Boolean expression using SOP by taking an example?

Q17. Explain Ripple counter and draw its logic diagram and timing diagram?

Q18. What are the types of digital to analog converter techniques? Explain R-2R ladder in detail?