Roll No. | | | | | | | | | | | | **Total No. of Pages : 03**

Total No. of Questions : 09

B.Tech.(CSE)/(IT) (Sem.–3)

DIGITAL CIRCUITS & LOGIC DESIGN

Subject Code : BTCS-303

M.Code : 56593

Date of Examination : 14-01-2023

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Answer following questions in brief :

a) How many states can an *n-bit* Ring counter and an *n-bit* Johnson's counter have?

b) What is octal representation of hexadecimal AFAFAF.

c) What are the advantages of ring counter?

d) What is difference between Moore and Mealy circuits?

e) What is EEPROM?

f) What is De-Morgan's law?

g) What is meant by the term edge triggered?

h) How many flip-flops are required to design a mod-7 up down counter?

i) Perform 2's complement subtraction of $(7)_{10} - (11)_{10}$.

j) What is race around condition? How it can be avoided?

SECTION-B

2. A ROM memory chip is rated at 4k × 8 bits. What, exactly, does this designation mean? How many addresses are there inside this memory chip? How many bits of storage are there, total, in this memory chip? How many address bits are there, and how many data bits are there?

3. Design an FPL A circuit, programmed to implement a 3- bit binary to Gray conversion.

4. Design a circuit that can be built using AOI (AND OR and Invertor) logic and output a 1 when a 4-bit BCD code is translated to a number that uses the upper right segment of a seven segment display. Show the truth table, K- map simplification and the logic diagram of the specified circuit.

5. Design a sequence detector to detect the sequence **1010** (overlapping of the sequence is permitted). Use D flip-flop to design the circuit. Show the intermediate design steps:

   a) State Diagram

   b) Truth Table/ Excitation table

   c) Logic Diagram of the circuit.

6. Prove the following identities using Boolean algebra

   $(A + B)(A + (AB)')C + A'(B + C) + A'B + ABC = C(A + B) + A'(B + C')$

SECTION-C

7. Using D-Flip Flops explain the working of a 4-bit Universal Shift Register.

8. A sequential circuit with two D flip-flops A and B, two inputs *x* and y, and one output z is specified by the following next-state and output equations

$$A(t + 1) = x'y + xB$$

$$B(t + 1) = x'A + xB$$

$$z = A$$

   a) Draw the logic diagram of the circuit.

   b) List the state table for sequential circuit.

   c) Draw the corresponding state diagram.

9. A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations

A is False, B is True

A is False, C is True

A, B, C are False

A, B, C are True

a) Write the Truth table for F. Use-the convention True = l and False = 0.

b) Write the simplified expression for F in SOP form.

c) Write the simplified expression for F in POS form.

d) Draw logic circuit using minimum number of 2-input NAND gates.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.